(variable threshold CMOS) is discussed. It should be noted that the term VTMOS is also referred to as a VTCMOS. The article in Appendix 3 by *Yang et al.* discloses the structure of a silicon-on- insulator-with-active-substrate (SOIAS) back-gate CMOS device which is a VTMOS. Appendix 4 contains an article by *Kachi et al.* which discloses the structure of a variable threshold-voltage SOI CMOSFET. Thus, all the articles in Appendix 2-4 disclose a VTMOS as described in *Kuroda et al.*, *I. Y. Yang et al.* and *Kachi et al.* which is different from the EIB of the present invention.

Claims 1, 6, 7 and 12 claim a MOS transistor and a method of controlling a threshold voltage of a MOS transistor by applying a voltage of a first polarity to a substrate for inducing charges of a second polarity over a composition surface of a surrounded (or body) region. Thus, by controlling the threshold voltage in accordance with a body bias, as claimed in claims 1, 6, 7 and 12, the claimed invention provides a MOS transistor and method thereof which are capable of operating a circuit at a high speed while reducing power consumption. The prior art does not show, teach or suggest applying a voltage of a first polarity to a substrate for inducing charges of a second polarity over a composition surface of a surrounded (or body) region as claimed in claims 1, 6, 7 and 12.

Claims 1, 2, 4-6, 7, 8 and 10-12 were rejected under 35 U.S.C. §103 as being unpatentable over *Burr* (U.S. Patent No. 6,100,567).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, it is respectfully requested that the Examiner withdraws the rejection to the claims and allows the claims to issue.

Burr appears to disclose a fully depleted silicon-on-insulator (SOI) device which includes an intrinsic channel region and a mechanism for tuning the threshold voltage thereof. (col. 1, lines 9-12) A "fully depleted" SOI device is shown in FIG. 3. Here, the device is configured such that the depletion regions 328 extend completely down to the interface with the oxide layer 308. The structure is otherwise similar to that of the partially depleted device, and includes an nfet 302 having source and drain n-regions 312 and 314, a p-type channel region 316, and a gate 318, and a pfet 304 having source and drain p-regions 320 and 322, an n-type channel region 324, and a gate 326. The substrate 310 is tied to a fixed potential such as ground. (col. 1, lines 48-59) Another configuration that has been proposed is shown in FIG. 5. Here, a first buried back gate p+ well 540 is formed within a p- substrate 510 beneath the nfet 518 (having n-type source and drain regions 512 and 514, a p-type channel region 516, and a gate 518), and a second buried back gate n+ well 542 is formed within the p- substrate beneath the pfet 504 (having p-type source and drains regions 520 and 522, an n-type channel region 524, and a gate 526). By providing separate contacts 544 and 546 in the conductive regions 540 and 542, respectively, separate bias potentials can be applied to the nfet 502 and pfet 504, thereby tuning the threshold voltage of each device. This approach has the advantage of avoiding the extra layers needed for the SOI AS structure, but suffers the drawback that it is only possible to decrease the threshold voltages slightly before forward biasing the p-n junction between the nfet and pfet back-gate wells, and thus the configuration of FIG. 5 cannot significantly reduce the threshold voltage, especially at low supply voltages. Further, the design is constrained by the diode leakage between the p and n conductive regions 540 and

542. For example, in the case where n-well bias potential is 0.6 volts less than the p-well bias potential, about 1 μA per micron of leakage will be present. These drawbacks are particularly acute for standard threshold devices when it is desired to reduce the threshold to an extremely low value. (col. 2, line 46 through col. 3, line 4)

Thus, *Burr* merely discloses a first buried back gate p+ well 540 and a second buried back gate n+ well 542 both formed within the p- substrate 510 and separate contacts 544 and 557 in the conductive regions 540 and 542 respectively, so that separate bias potentials are applied. In other words, *Burr* teaches that the bias is provided to the buried back gate wells 540, 542 in *Burr*. Thus nothing in *Burr* shows, teaches or suggests applying a voltage of a first polarity to a substrate as claimed in claims 1, 6, 7 and 12. Rather, the bias in *Burr* is provided to the buried back gate wells 540, 542 via contacts 544 and 546.

Additionally, *Burr* merely discloses that the threshold voltage is only slightly decreased before forward bias of the p-n junction between the back-gate wells and in addition there is diode leakage between the p and n conductive regions 540 and 542. Thus nothing in *Burr* shows, teaches or suggests inducing charges of a second polarity over the composition surface of the surrounded or body region as claimed in claims 1, 6, 7 and 12. Rather, *Burr* merely discloses forward biasing the p-n junction between the back-gate wells and the diode leakage between the p and n conductive regions 540 and 542.

Since nothing in *Burr* shows, teaches or suggests a) a substrate is applied with a voltage of a first polarity or b) inducing charges of a second polarity over the composition surface of the body region due to the first polarity voltage applied to the substrate as

claimed in claims 1, 6, 7 and 12, it is respectively requested that the Examiner withdraws the rejection to claims 1, 6, 7 and 12 under 35 U.S.C. §103.

Claims 2, 4-5, 8 and 10-11 depend from claims 1 and 7 and recite additional features. It is respectfully submitted that claims 2, 4-5, 8 and 10-11 would not have been obvious over *Burr* within the meaning of 35 U.S.C. §103 at least for the reasons as set forth above. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claims 2, 4-5, 8 and 10-11 under 35 U.S.C. §103.

Claims 3 and 9 were rejected under 35 U.S.C. §103 as being unpatentable over *Burr* in view of *Warashina et al.* (U.S. Patent No. 5,698,885).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §103. The claim has been reviewed in light of the Office Action, and for reasons which will be set forth below, it is respectfully requested that the Examiner withdraws the rejection to the claim and allows the claim to issue.

As discussed above, nothing in *Burr* shows, teaches or suggests the primary features of the claimed invention. It is respectfully submitted that secondary reference will not overcome the deficiencies in the primary reference. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claims 3 and 9 under 35 U.S.C. §103.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested. Should the Examiner find that the application is not now in condition for allowance, it is respectfully requested that the Examiner enters this amendment for purposes of Appeal.

If for any reason Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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